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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,382	02/27/2004	Gerry Ashton	BUR920020128US1	2381

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EXAMINER	
MERANT, GUERRIER	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,382	ASHTON ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/30/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/30/07* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendment filed 03/30/07 have been fully considered but they are not persuasive.

Response to Arguments

Applicants contend that "**Gregor et al.** do not disclose or suggest at least one shift register latch, comprising.., a first latch.., an input for receiving a first clock signal; and.., a circuit, connected between said input and said first latch configured for generating a second clock signal .... ". The Examiner respectfully disagrees. **Gregor et al.** clearly discloses an integrated circuit, comprising:

a) a first clock tree *(item 1110, Fig. 11)* for receiving a first clock signal having a plurality of pulses each having a first width

a) at *least* one shift register latch *(item 1140, Figs. 11 &12)*, comprising:

i) a first latch *(item 1520)*;

ii) a second latch *(item 1530)* in electrical communication with said first latch;

iii) an input for receiving a first clock signal *(Single Clock, Fig. 11)*;

iv) and a circuit *(item 140, Fig.2)*, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal *(col. 4, lines 20-25)*.

The Examiner notes that in the previous Office Action *the circuit connected between said input and said first latch* was wrongly cited as *(item 1130, Fig.11) instead of item 140, fig. 2.*

Furthermore, Applicants argue, "Gregor et al. shift register latch in fact does not contain a second-clock-signal generating circuit" and "that the shift register latch itself have an input and contain the first latch. It also requires that the shift register latch contain the second-clock-generating circuit between the input and the first latch." The Examiner notes these limitations are not recited in the rejected claims (s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. *See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).*

Due to the reasons state above, the Examiner maintains rejections with respect to claims 1-20. Gregor et al. discloses all the limitations that the Applicant suggests distinguish from the prior art. Therefore, claims 1-20 are not patentably distinct or non-obvious over the prior art of record as presented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-7, 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by **Gregor et al. (US 6,304,122)**.

Claims 1, 2, 7: **Gregor et al.** discloses an integrated circuit, comprising:

a) a first clock tree *(item 1110, Fig. 11)* for receiving a first clock signal having a plurality of pulses each having a first width

a) at *least* one shift register latch *(item 1140, Figs. 11 &12)*, comprising:

i) a first latch *(item 1520)*;

ii) a second latch *(item 1530)* in electrical communication with said first latch;

iii) an input for receiving a first clock signal *(Single Clock, Fig. 11)*;

iv) and a circuit *(item 140, Fig.2)*, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal *(col. 4, lines 20-25)*.

Claim 3: **Gregor et al.** discloses an integrated circuit according as in claim 1 above, wherein said circuit comprises a pulse generator for generating a first clock pulse for said first latch *(Single Clock, Fig. 11)*.

Claims 5 and 6: **Gregor et al.** discloses an integrated circuit according as in claim 1 above, wherein said first clock signal comprises a plurality of first pulses each having a first duration and said second clock signal comprises a plurality of second pulses each having a second duration shorter than said first duration *(col. 8, lines 6-20; Fig. 13)*.

Claim 10: **Gregor et al.** discloses an integrated circuit according as in claim 7 above, further comprising a multiplexer *(item 1510; Fig. 15)* in electrical communication with said master latch *(item 1520; Fig. 15)*.

Claims 11-13: **Gregor et al.** discloses an integrated circuit according as in claim 7 above, comprising at least one first scan chain *(SRL 1140 would be serially connected to other SRLs through the SO output. The L1 and L2 outputs would be sent to the appropriate logic that uses these values meaning they are second, third, or fourth scan chains- col. 8, lines 31-34- see Figs. 11 & 15)* comprising a plurality of first shift register latches *(items 1520 & 1530; Fig. 15)*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 8 and 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregor et al.** and further in view of **Joordens et al. (US 2004/0061539)**.

Claims 4, 8 and 9: **Gregor et al.** substantially teaches an integrated circuit according to claims 3 and 7 above, wherein said pulse generator comprises inverters and transistors *(see Fig. 12)* and fails to disclose fails to disclose an AND gate and an inverter instead of inverters and transistors. However, **Joordens et al.** teaches a phase detector circuit comprising an inverter *(item 720)* and a NAND gate *(AND gate & inverter item 740) (see Figs. 7 & 8) that detects rising edges of the data and clock. In another embodiment according to the present invention, the phase detector may be designed to detect data transitions outside of the window as well (i.e., on the falling edge of the clock). Any mismatch between the rising and the falling edge is filtered out (by the loop) [0044]. Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to use the phase detector circuit of* ***Joordens et al****. to acquire distorted signals at very high data rates and to provide a clock signal and retimed or recovered data as outputs [005-006;* ***Joordens et al****.] because clock recovery is often essential for the regeneration of distorted binary sigals [0007;* ***Joordens et al****.].*

Claims 14 and 15: **Gregor et al.** substantially teaches an integrated circuit including: a) a scan clock tree *(item 1110, Fig. 11)* for receiving a first clock signal having a plurality of pulses each having a first width

a) at *least* one shift register latch *(item 1140, Figs. 11 &12)*, comprising:

i) a first latch *(item 1520)*;

ii) a second latch *(item 1530)* in electrical communication with said first latch;

iii) an input for receiving a first clock signal *(Single Clock, Fig. 11)*;

iv) and a circuit *(item 140, Fig.2)*, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal *(col. 4, lines 20-25)*. But **Gregor et al.** fails to teach a power supply connected to the integrated circuit. However, ***Joordens et al*** teaches a phase detector circuit comprising a power supply *(charge pump, item 920; FiG. 9) that takes an input from a phase detector (item 910), sends the output to a low-pass filter (item 930) which generates the oscillator control voltage that the sets the VCO (item 940) in order to reduce jitter [0046].* Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious *to use the power supply (charge pump) disclosed in* **Joordens et al.** *to integrate the phase difference between up and down on a loop filter capacitance and translates a phase error into a voltage difference [0039;* ***Joordens et al****.].*

Claim 16: **Gregor et al.** and **Joordens et al.** teache an integrated circuit according as in claim 14 above, wherein said circuit comprises a pulse generator for generating a first clock pulse for said first latch *(Single Clock, Fig. 11)*.

Claims 17: **Gregor et al.** and **Joordens et al.** teache an integrated circuit according to claims16 above, wherein said pulse generator comprises inverters and transistors *(see Fig. 12)* and fails to disclose fails to disclose an AND gate and an inverter instead of inverters and transistors. However, **Joordens et al.** teaches a phase detector circuit comprising an inverter *(item 720)* and a NAND gate *(AND gate & inverter item 740) (see*

Figs. 7 & 8) that detects rising edges of the data and clock. In another embodiment according to the present invention, the phase detector may be designed to detect data transitions outside of the window as well (i.e., on the falling edge of the clock). Any mismatch between the rising and the falling edge is filtered out (by the loop) [0044]. Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to use the phase detector circuit of ***Joordens et al****. to acquire distorted signals at very high data rates and to provide a clock signal and retimed or recovered data as outputs [005-006;* ***Joordens et al****.] because clock recovery is often essential for the regeneration of distorted binary sigals [0007;* ***Joordens et al****.].*

Claims 18 and 19: **Gregor et al.** teaches an integrated circuit according as in claim 14 above, wherein said first clock signal comprises a plurality of first pulses each having a first duration and said second clock signal comprises a plurality of second pulses each having a second duration shorter than said first duration *(col. 8, lines 6-20; Fig. 13)*.

Claim 20: **Gregor et al.** teaches an integrated circuit according as in claim 14 above, further comprising a multiplexer *(item 1510; Fig. 15)* in electrical communication with said master latch *(item 1520; Fig. 15)*.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

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Merant Guerrier
06/08/07

Cynthia Britt
CYNTHIA BRITT
PRIMARY EXAMINER
6-7-07